Pending Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously presented) A method of maintaining execution threads in a parallel multithreaded processor comprises:

accessing, by a thread executing in the multithreaded processor, a register in a register set organized into a plurality of windows of registers, each of the plurality of windows of registers associated with a corresponding thread, each register in the plurality of windows of registers being relatively addressable by the corresponding thread and absolutely addressable by two or more of the threads executing on the multithreaded processor with absolutely addressable comprises providing an exact address of the register with the exact address specified in an instruction.

2. (Original) The method of claim 1 wherein multiple threads can use the same control store and relative register locations but access different window banks of registers.

3. (Original) The method of claim 1 wherein the relative register addressing divides the register banks into windows across the address width of the general purpose register set.

4. (Original) The method of claim 1 wherein relative addressing allows access any of the window registers relative to the starting point of a window of registers.

5. (Original) The method of claim 1 further comprising:

organizing the register set into windows according to the number of threads that execute in the processor.

6. (Original) The method of claim 1 wherein relative addressing allow the multiple threads to use the same control store and locations while allowing access to different windows of register and perform different functions.

7. (Original) The method of claim 1 wherein the window registers are implemented using dual ported random access memories.

8. (Original) The method of claim 1 wherein relative addressing allows access to any of the windows of registers relative to the starting point of the window of registers.

9. (Cancelled)

10. (Previously presented) The method of claim 1 wherein the exact address of the register is directly specified in a source field or destination field of the instruction.

11. (Original) The method of claim 1 wherein relative addresses are specified in instructions as an address offset within a context execution space as defined by a source field or destination field operand.

12. (Previously presented) A hardware based multi-threaded processor comprises:

a processor unit comprising:

control logic circuit including context event switching logic, the context switching logic arbitrating access to the microengine for a plurality of executable threads;

an arithmetic logic unit to process data for executing threads; and

a register set that is organized into a plurality of windows of registers, each of the plurality of windows of registers associated with a corresponding one of the plurality of threads,

each register in the plurality of windows of registers being relatively addressable by the corresponding thread associated with the respective window of registers and absolutely addressable by two or more of the threads executing on the multi-threaded processor, with any one of the registers of the register set being absolutely addressable by providing an exact address of the register with the exact address specified in an instruction.

13. (Previously presented) The processor of claim 12 wherein the control logic circuit further comprises:

an instruction decoder; and

program counter units to track executing threads.

14. (Original) The processor of claim 13 wherein the program counters units are maintained in hardware.

15. (Previously presented) The processor of claim 12 wherein the register set is organized into windows across an address width of the general purpose register set with each window relatively accessible by the corresponding thread.

16. (Original) The processor of claim 15 wherein the relative addressing allows access to any of the registers relative to the starting point of a window of registers.

17. (Original) The processor of claim 15 wherein the number of windows of the register set is according to the number of threads that execute in the processor.

18. (Previously presented) The processor of claim 12 wherein relative addressing allow the multiple threads to use the same control store and locations while allowing access to different windows of register and perform different functions.

19. (Previously presented) The processor of claim 12 wherein the windows of registers are provided using dual ported random access memories.

20. (Original) The processor of claim 12 wherein the processing unit is a microprogrammed processor unit.

21. (Previously presented) A computer program product residing on a computer readable storage medium for managing execution of multiple threads in a multithreaded processor comprising instructions causing a processor to:

access, by an executing thread in the multithreaded processor, a register in a register set organized into a plurality of windows of registers, each of the plurality of windows of registers being associated with a corresponding thread, each register in the plurality of windows of registers being relatively addressable by the corresponding thread and absolutely addressable by two or more threads executing on the multithreaded processor with absolutely addressable comprises instructions that when executed cause the processor to provide an exact address of the register with the exact address specified in an instruction.

22. (Cancelled)